10% of V_{dd} to 90% of V_{dd} or falls from 90% of V_{dd} to 10% of V_{dd}. For the example in Figure 1, the driving instance delay is the time delay exhibited by driver 110 to propagate a signal as measured by the time difference required to generate a voltage, V_d, at the output of driver 110 from an input voltage in input vector 105. The gate level circuit (*e.g.*, driver 110) may include one or more inputs. The input vectors represent the combinations of different inputs states. The example of Figure 1 has only one input signal that transitions from 0 to 1 or from 1 to 0, thereby causing the output signal to switch from 1 to 0 or 0 to 1, respectively. For the simplified driver circuit of Figure 1, which includes only one input, input vectors 105 include one input waveform that transitions from a low logic level to a high logic level, and a second input vector that transitions from a high logic level to a low logic level. As described below in conjunction with Figure 2, the circuit may include multiple inputs, and the input vectors may include different combinations of signal transitions for the multiple inputs.

IN THE CLAIMS:

Please amend claims 10, 22 and 24 as follows:

10. (Once Amended) A method for characterizing a circuit for determining a timing delay, said method comprising the step of:

determining a resistive-capacitive ("RC") network between a driving point and a receiving point, said circuit driving said RC network at said driving point;

selecting a plurality of time instances for analysis of said circuit;